What is claimed is:

1. A transistor array, comprising:

a plurality of LSB transistors arranged along diagonal directions of a central portion of an array including a plurality of rows and a plurality of columns; and

a plurality of MSB transistors arranged along diagonal directions above and below the plurality of LSB transistors, respectively.

2. The transistor array of Claim 1, wherein each of the plurality of MSB transistors includes a plurality of transistors having the same size as an LSB transistor.

3. The transistor array of Claim 1, wherein among the plurality of MSB transistors, the MSB transistors above the LSB transistors are arranged in increasing numerical order (e.g., M1, M2, etc.) from the diagonal direction areas close to the plurality of LSB transistors to an edge area, and the MSB transistors below the LSB transistors are arranged reversely or in a decreasing numerical order (e.g., M15, M14, etc.) from the diagonal direction areas close to the plurality of LSB transistors to an edge area.

4. A transistor array, comprising:

a plurality of first LSB transistors arranged along diagonal directions of a central portion of a first quadrant of an array including a plurality of rows and a plurality of columns;

a plurality of first MSB transistors arranged along diagonal directions respectively above and below the plurality of first LSB transistors;

a plurality of second LSB transistors and a plurality of second MSB transistors arranged on a second quadrant of the array to be symmetrical in a Y-axis direction to the plurality of first LSB transistors and the plurality of first MSB transistors;

a plurality of third LSB transistors and a plurality of third MSB transistors arranged on a third quadrant of the array to be symmetrical in an X-axis direction to the plurality of first LSB transistors and the plurality of first MSB transistors; and

a plurality of fourth LSB transistors and a plurality of fourth MSB transistors arranged on a fourth quadrant of the array to be symmetrical in a Y-axis direction to the plurality of third LSB transistors and the plurality of third MSB transistors.

5. The transistor array of Claim 4, wherein each of the plurality of first to fourth MSB transistors includes a plurality of transistors having the same size as the LSB transistors.

6. The transistor array of Claim 4, wherein among the plurality of first MSB transistors, the first MSB transistors above the plurality of first LSB transistors are arranged in order from the diagonal direction areas close to the plurality of LSB transistors to an edge area, and the first MSB transistors below the LSB transistors are arranged reversely from the diagonal direction areas close to the plurality of LSB transistors to an edge area.

7. A layout method of a transistor array, comprising:

arranging a plurality of LSB transistors along diagonal directions of a central portion of an array including a plurality of rows and a plurlity of columns; and

arranging a plurality of MSB transistors, respectively, along diagonal directions above and below the plurality of LSB transistors.

8. The method of Claim 7, wherein each of the plurality of MSB transistors includes a plurality of transistors having the same size as the LSB transistors.

9. The method of Claim 7, wherein the step of arranging the plurality of MSB transistor includes:

arranging the MSB transistors above the LSB transistors in order from the diagonal direction areas close to the plurality of LSB transistors to an edge area; and

arranging the MSB transistors below the LSB transistors reversely from the diagonal direction areas close to the plurality of LSB transistors to an edge area.

10. A layout method of a transistor array, comprising:

arranging a plurality of first LSB transistors along diagonal directions of a central portion of a first quadrant of an array including a plurality of rows and a plurality of columns;

arranging a plurality of first MSB transistors along diagonal directions above and below the plurality of first LSB transistors, respectively;

arranging a plurality of second LSB transistors and a plurality of second MSB transistors on a second quadrant of the array to be symmetrical in a Y-axis direction to the plurality of first LSB transistors and the plurality of first MSB transistors;

arranging a plurality of third LSB transistors and a plurality of third MSB transistors on a third quadrant of the array to be symmetrical in an X-axis direction to the plurality of first LSB transistors and the plurality of first MSB transistors; and

arranging a plurality of fourth LSB transistors and a plurality of fourth MSB transistors on a fourth quadrant of the array to be symmetrical in a Y-axis direction to the plurality of third LSB transistors and the plurality of third MSB transistors.

11. The method of Claim 10, wherein each of the plurality of first to fourth MSB transistors includes a plurality of transistors having the same size as the LSB transistors.

12. The method of Claim 10, wherein the step of arranging the plurality of first MSB transistors includes:

arranging the first MSB transistors above the plurality of first LSB transistors in order from the diagonal direction areas close to the plurality of LSB transistors to an edge area; and

arranging the first MSB transistors below the LSB transistors reversely from the diagonal direction areas close to the plurality of LSB transistors to an edge area.

13. A transistor array comprising:

a plurality of first transistors arranged along a diagonal direction of a central portion of an array; and

a plurality of second or compound transistors, each compound transistor comprising a plurality of component transistors arranged with component transistors of each compound transistor disposed along diagonal directions both above and below the plurality of first transistors, respectively.

14. The transistor array of Claim 13 wherein the plurality of second transistors disposed above the plurality of first transistors are arranged in increasing numerical order from the diagonal direction areas close to the plurality of first transistors to an edge area, and the plurality of second transistors below the plurality of first transistors are arranged reversely or in a decreasing numerical order from the diagonal direction areas close to the plurality of first transistors to an edge area.

15. The transistor array of Claim 14 wherein said transistor array defines a first quadrant of a larger array, said larger array further comprising second, third and fourth quadrants disposed adjacent to the first quadrant and arranged such that the second quadrant is symmetric in a Y-axis direction to the transistor array of the first quadrant, the third quadrant is symmetric in an X-axis direction to the transistor array of the first quadrant, and the fourth quadrant is symmetric in a Y-axis direction to the transistor array of the third quadrant.

16. The transistor array of Claim 15 wherein the larger array comprises a transistor array arranged in consideration of error values such that an error value of each of the plurality of first transistors is about zero, and the sum totals of error values of a plurality of component transistors which constitute each of the second or compound transistors is about zero.

17. The transistor array of Claim 13 wherein each of the plurality of first transistors comprises a less-significant-bit transistor, and each of the plurality of second transistors comprises a more-significant-bit transistor.

18. The transistor array of Claim 13 wherein the array implements a digital-to-analog conversion circuit.

19. The transistor array of Claim 14 wherein the numerical order corresponds to the magnitude of significance of a bit position.

20. The transistor array of Claim 16 wherein the error values have normalized weighting with respect to the error values of the plurality of first transistors.